CLAIMS:

1. A method for operating a pump circuit of a memory device comprising:

activating a first plurality of parallel voltage pumps while an output count of a counter circuit is equal to or less than a predetermined quantity of pulses, such that the activated pumps provides an output voltage with a first current limit; and

activating the first plurality of pumps and a second plurality of pumps while an output count of the counter circuit is greater than the predetermined quantity of pulses, such that the first and second pumps provide the first output voltage with a second current limit that is greater than the first current limit.

2. The method of claim 1 wherein the output count is a provided by a pulse counter of the memory device.

3. The method of claim 1 wherein the memory device is a flash memory device, and the first output voltage is coupled to a source node of floating gate memory devices during an erase operation.

4. The method of claim 1 wherein the first and second plurality of pumps are selectively activated to increase a cumulative output current of the first and second plurality of pumps in response to an increasing running count of the counter circuit.

5. The method of claim 1 wherein the output voltage is 12V.

6. The method of claim 1 wherein the predetermined quantity of counts is 1000.

7. A method for erasing a flash memory cell comprising:

applying a negative voltage to a control gate of the flash memory cell; and

applying a series of positive voltage pulses to a source of the flash memory cell, wherein a current limit of the positive voltage pulses increases based upon the number of positive voltage pulses applied.

8. The method of claim 7 wherein the negative voltage is about -10 volts, and the positive voltage pulses have a potential up to about 5 volts.

9. The method of claim 7 wherein the potential of the positive voltage pulses is generated using parallel voltage pump circuits each having a plurality of series coupled pump stages.

10. The method of claim 9 wherein the parallel voltage pump circuits are selectively activated using an output count of a pulse counter.

11. The method of claim 7 and further including applying a ground potential to a substrate of the memory cell while a drain connection is floating.

12. The method of claim 7 wherein the negative voltage is in a range of –10 to –17V.

13. A method for erasing a flash memory cell having a control gate, a source connection, a drain connection, and a floating gate for storing a charge to be erased, the method comprising:

applying a negative voltage to the control gate of the flash memory cell, the negative voltage being larger than a supply voltage; and

applying a series of positive voltage pulses to the source connection of the flash memory cell, wherein a current limit of the positive voltage pulses increases based upon the quantity of positive voltage pulses applied.

14. The method of claim 13 and further including allowing the drain connection to float.

15. The method of claim 13 and further including verifying erase of the flash memory cell.

16. The method of claim 13 wherein each positive voltage pulse is in a range of tens of milliseconds in length.

17. The method of claim 13 wherein the quantity of positive voltage pulses are less than 1000.

18. The method of claim 13 wherein an electric field in the floating gate to source causes a breakdown in a depletion region of the memory cell.

19. The method of claim 13 wherein as the memory cell becomes more erased, the negative voltage on the control gate becomes less negative and a gate induced drain leakage current decreases.

20. The method of claim 13 wherein the voltage pump provides an output voltage greater than a supply voltage.